WT6630P
USB Power Delivery Controller

Data Sheet

Rev. 1.05

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Table of Contents

1. General Description

The WT6630P is an USB Power Delivery (PD) controller designed for USB Type-C adapter or charger. It integrates USB PD baseband PHY, Type-C cable detection, shunt regulator, voltage and current monitor, 8-bit MCU and control circuit of blocking MOSFET. An One-Time-Programmable (OTP) ROM is provided for program code and user configuration data.

To minimize external components, an on-chip regulator provides 1.8V for MCU and can operate at single power supply from 4V to 30V.

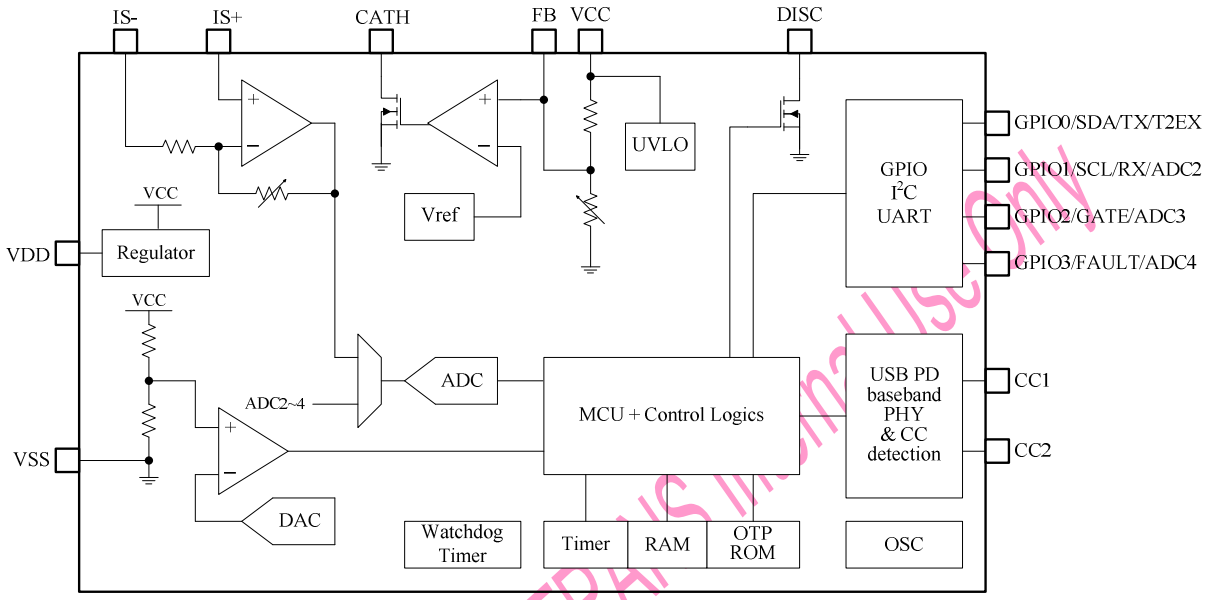
2. Features

- USB Type-C charge-only Downstream Facing Port (DFP)
- USB Power Delivery Rev.2.0 baseband communication
- Built-in shunt regulator and support 5V to 20V VBUS output
- Programmable Over Voltage Protection (OVP) and Over Current Protection (OCP)
- Low side voltage output current shunt monitor
- 10-bit ADC for voltage and current monitoring
- 8-bit MCU
  - implements Power Delivery message protocol and device policy
  - VBUS output control
  - power supply protection
- 8k bytes One-Time-Programmable (OTP) ROM
- 512 bytes RAM
- External blocking MOSFET control
- Internal RC oscillator
- Internal VDD regulator
- General purpose I/Os
- Serial interface: I^2C and UART
- Support power saving mode
- Operating voltage range: 4V ~ 30V
- Operating temperature range: -20℃ ~ +105℃
- Package (Green Package): 14-pin SOP, 16-pin QFN

Application :

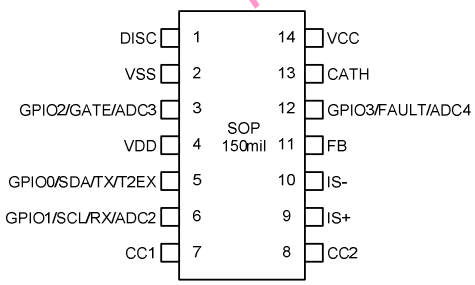
- USB Type-C AC adapters and chargers

3. Block Diagram

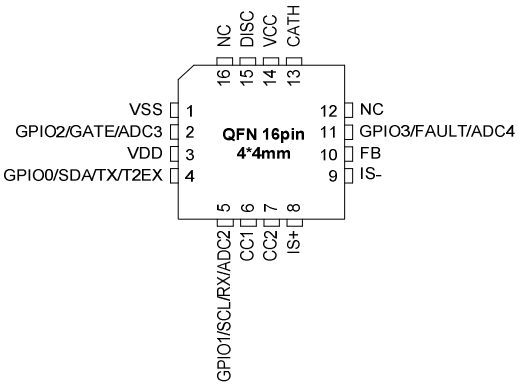


4. Pin Configuration

14-pin SOP



16-pin QFN



4.1 Pin Description

Pin Number		Pin Name	Function	I/O Voltage	Type		Description
SOP14	QFN16				Input	Output	
1	15	DISC	DISC	HV	-	OD	Discharge
2	1	VSS	VSS	-			Ground
3	2	GPIO2/GATE/ ADC3	GPIO2	HV	TTL	PP	General purpose I/O.
			GATE		-	PP	Blocking MOS Control
			ADC3		AN	-	ADC input
4	3	VDD	VDD	-	-	AN	Regulator output
5	4	GPIO0/SDA/ TX/T2EX	GPIO0	HV	TTL	OD	General purpose I/O.
			SDA		TTL	OD	I^2C data
			TX		-	OD	UART transmitter
			T2EX		TTL	-	Timer2 capture mode input
6	5	GPIO1/SCL/ RX/ADC2	GPIO1	LV	TTL	OD	General purpose I/O.
			SCL		TTL	OD	I^2C clock
			RX		TTL	-	UART receiver
			ADC2		AN	-	ADC input
7	6	CC1	CC1	HV	CC	PP	USB Type-C Configuration Channel
8	7	CC2	CC2	HV	CC	PP	USB Type-C Configuration Channel
9	8	IS+	IS+	LV	AN	-	Positive input of current sensing amplifier.
10	9	IS-	IS-	LV	AN	-	Negative input of current sensing amplifier.
11	10	FB	FB	LV	AN	-	Feedback of shunt regulator
12	11	GPIO3/FAULT /ADC4	GPIO3	HV	TTL	OD	General purpose I/O. Open drain output.
			FAULT		-	OD	Fault indication. Outputs low when OVP/OCP.
			ADC4		AN	-	ADC input
13	13	CATH	CATH	HV	-	AN	Cathode of shunt regulator
14	14	VCC	VCC	HV	-	-	Positive power supply

Legend: HV = High Voltage (max. 30V), LV = Low voltage (max. 4.5V), OD = Open Drain, PP = Push Pull, AN = analog, TTL = TTL compatible input, CC = USB PD baseband input.

5. Functional Descriptions

5.1 Shunt Regulator

VBUS output voltage can be controlled by programming the ratio of resistors and is illustrated in Fig.5.1. It supports 5V, 9V, 12V, 15V, 17V, 19.5V and 20V VBUS output. Default is 5V after power on.

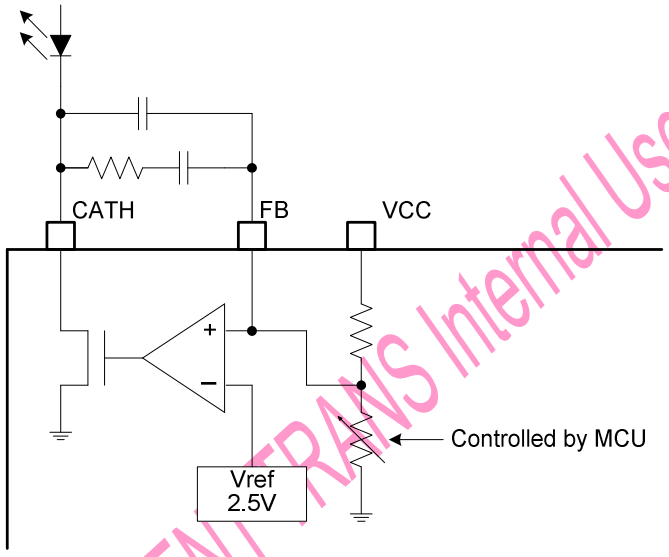


Fig. 5.1 VBUS voltage control

5.2 Over Voltage Protection (OVP)

Over voltage protection is implemented by a comparator and a 10-bit DAC (Digital to Analog Converter). When VCC voltage is larger than the OVP trip point which is set by DAC, GATE pin goes to high level to turn off blocking MOSFET and generates an interrupt to MCU.

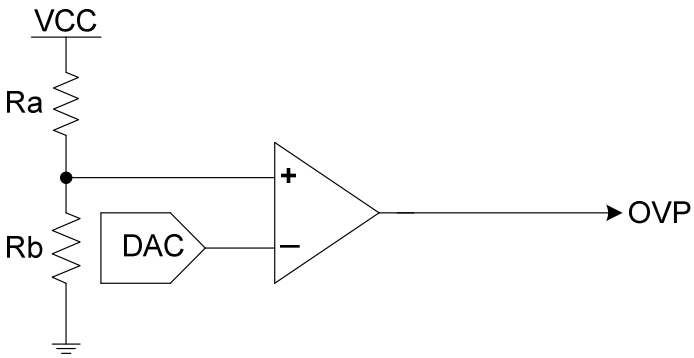


Fig. 5.2 OVP circuit

5.3 Low Side Current Shunt Monitor and OCP

Load current is sensed by amplifying the voltage drop across the shunt resistor at low side. MCU can read the load current through ADC and generate the over current protection (OCP). The gain of amplifiers are programmable from 20 to 100.

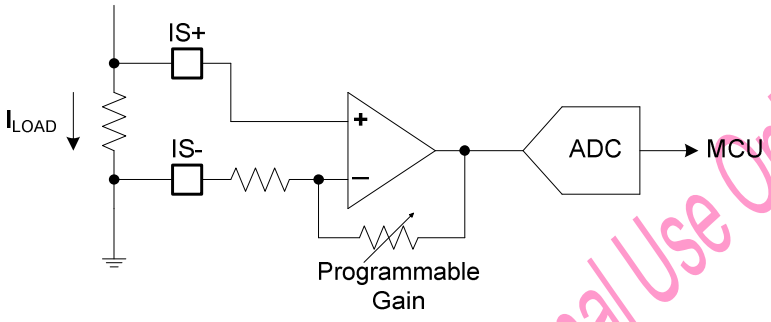


Fig. 5.3 Load current monitor

5.4 USB Type-C and Power Delivery

CC Termination and connection detect

The termination is implemented by a selectable current source, I_{RP_CC} , which is 80, 180, or 330μA. By monitoring the CC1 and CC2 voltage, it can detect a UFP is attached or not.

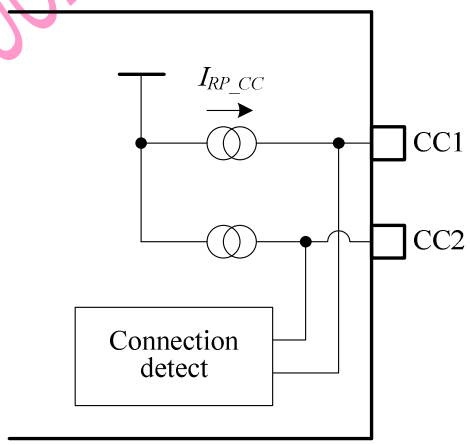


Fig. 5.4 CC1 and CC2 pull-up and detection

When UPF is attached, GATE pin goes to low and turn on blocking MOSFET.

When UPF is detached, GATE pin goes to high level and turn off blocking MOSFET.

USB PD PHY

USB PD PHY consists of a pair of transmitter and receiver that communicate across CC wire using Biphase Marking Coding (BMC).

The transmitter performs :

- Receive packet data from the protocol layer
- Calculate and append a CRC
- Encode the packet data including the CRC
- Transmit the Packet (Preamble, SOP, payload, CRC and EOP) across the CC channel using BMC

The receiver performs :

- Recover the clock and lock onto the Packet from the Preamble
- Detect the SOP
- Decode the received data including the CRC
- Detect the EOP and validate the CRC
- If the CRC is valid, deliver the packet data to the protocol layer.
- If the CRC is not valid, flush the received data

5.5 Discharge

When VBUS transits from a higher voltage level to a lower voltage level, it requires a discharge current to fulfill the transition time specification of USB-PD. There are four transistors can be enabled independently to control discharge time. Care must be taken when discharging with large current at high voltage level.

5.6 MCU and Peripherals

MCU

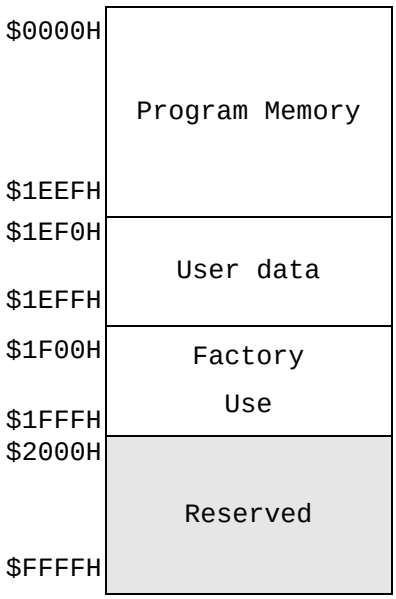
Embedded turbo 8051 compatible CPU with 16-bit address bus and 8-bit data bus. Maximum operating frequency is 10 MHz.

RAM

The data memory is divided into two blocks: one is internal 256 bytes SRAM and the other is on-chip external 256 bytes SRAM.

OTP Memory

One-Time-Programmable Memory is 8k bytes. A 256 bytes space is reserved for user data.



Timer/Counter

Two 16-bit Timer/Counters are provided. All two Time/Counter can be configured as Timer or Counter.

Serial interfaces

UART: Standard 8052 UART, support baud rate up to 115200 at oscillator = 10 MHz.

I^2C: Slave mode only I^2C for data communication

GPIO

General purpose I/O pin is controlled by MCU. When set as an output, it is an open drain output.

Watchdog timer

The watchdog timer is a programmable timer that generates a RESET if the MCU does not clear it before time out. The clock source of watchdog timer is from an independent low frequency oscillator.

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Parameter		Min.	Max.	Units
Supply voltage VCC pin		–0.3	30	V
Input voltage	CATH, CC1, CC2	–0.3	VCC + 0.3 (max. 30V)	V
	FB, IS+, IS-	–0.3	5.5	V
Output voltage	DISC, GPIO0, GATE/GPIO2, FAULT/GPIO3	–0.3	VCC + 0.3 (max. 30V)	V
	GPIO1	–0.3	5.5	V
	VDD	–0.3	3	V
Operating temperature		-40	125	℃
Storage temperature		-55	150	℃

NOTE: Maximum ratings applied to the device are individual stress limit value. Stresses above those listed may cause permanent damage and reliability may be affected.

6.2 Recommended Operating Parameters

Parameter		Condition	Min.	Typ.	Max.	Units
V_{CC_OPR}	Operating voltage		4		30	V
V_{FB}	Feedback of shunt regulator		-0.3		4.5	V
V_{IN}	IS+ and IS- input voltage range		-0.3		4.5	V
T_{OPR}	Operating Temperature		-20		105	℃

6.3 DC Electrical Characteristics (VCC = 20V, Ta = -20 ~ +105°C, unless specified)

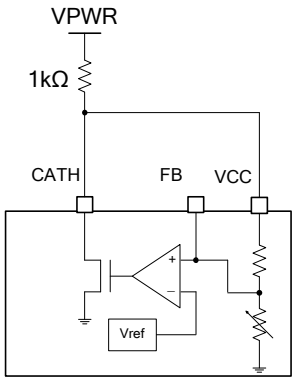
VCC and VDD

Parameter		Condition	Min.	Typ.	Max.	Units
V_{CC}	VCC Operating Voltage		4		30	V
I_{CC_OPR}	VCC Current, normal operating	No load at output and MCU operating @ 10MHz		1.5	3	mA
I_{CC_SLEEP}	VCC Current, sleep mode	CC1 pin floating		0.8	1.0	mA
		CC1 pin 5.1KΩ pull low			1.3	mA
V_{UVLO}	VCC Under Voltage Lockout	VCC rising			3.8	V
		VCC falling	3.2			V
I_{DISC}	VCC discharge current	VCC = 8V, DISC_CTL= 0001	52	80	108	mA
		VCC = 8V, DISC_CTL= 0010	59	90	122	mA
		VCC = 8V, DISC_CTL= 0100	65	100	135	mA
		VCC = 8V, DISC_CTL = 1000	75	115	155	mA
V_{DD}	VDD regulator output voltage		1.75	1.85	1.95	V

Shunt regulator

Parameter		Condition	Min.	Typ.	Max.	Units
V_{REF}	Reference voltage	V_{CATH} = V_{FB} and I_{CATH} = 1mA Ta = 25℃	2.49	2.5	2.51	V
		V_{CATH} = V_{FB} and I_{CATH} = 1mA Ta = -20℃ ~ +105℃	2.48	2.5	2.52	V
V_{OUT}	Regulator output voltage*(1)	VPWR = 8V, 5V output	4.9	5	5.1	V
		VPWR = 15V, 12V output	11.64	12	12.36	V
		VPWR = 23V, 20V output	19.4	20	20.6	V

*(1) Regulator output voltage test circuit



Over Voltage Protection (OVP)

Parameter		Condition	Min.	Typ.	Max.	Units
E_{OVP}	OVP trip point error	VCC > 5V, V_{REF_OVP} = 1.8V			±150	mV
V_{REF_OVP}	Reference voltage of DAC	Ta = 25℃, VCC = 5V	1.79	1.8	1.81	V

ADC

Parameter		Condition	Min.	Typ.	Max.	Units
N_{ADC}	ADC resolution			10		bit
INL_{ADC}	ADC INL	V_{REF_ADC} = 1.8V			±5	LSB
DNL_{ADC}	ADC DNL	V_{REF_ADC} = 1.8V			±5	LSB
V_{REF_ADC}	Reference voltage of ADC	Ta = 25℃, VCC = 5V	1.79	1.8	1.81	V

CC1 and CC2

Parameter		Condition	Min.	Typ.	Max.	Units
V_{OH_CC}	Output high voltage of BMC transmitter		1.05	1.125	1.2	V
V_{OL_CC}	Output low voltage of BMC transmitter		0		0.075	V
V_{IH_CC}	Input high voltage of BMC receiver		0.67		1.45	V
V_{IL_CC}	Input low voltage of BMC receiver		-0.25		0.43	V
Z_{DRIVER_CC}	BMC Transmitter output impedance		33		75	Ω
I_{RP_CC}	CC1 and CC2 pull-up current	Capability 0.5A @5V	64	80	96	μA
		Capability 1.5A @5V	166	180	194	μA
		Capability 3.0A @5V	304	330	356	μA
V_{Rd_CC}	CC1 and CC2 attachment detection threshold	Capability 0.5A @5V	1.5	1.6	1.65	V
		Capability 1.5A @5V	1.5	1.6	1.65	V
		Capability 3.0A @5V	2.45	2.6	2.75	V

GPIO

Parameter		Condition	Min.	Typ.	Max.	Units
V_{OL_GPIO1}	Output Low Voltage of GPIO1	I_{OL} = 4 mA			0.4	V
V_{OL_GPIOx}	Output Low Voltage of GPIO0, GPIO2 and GPIO3	I_{OL} = 10 mA			0.4	V
V_{OH_GPIO2}	Output High Voltage of GPIO2	I_{OH} = 10 mA	V_{CC} -0.4			V
I_{Z_GPIO}	Leakage current of GPIO in Hi-Z				10	μA
V_{IH}	Input high voltage	GPIO1	1.4		4.5	V
		GPIO0, GPIO2, GPIO3	1.4		VCC	V
V_{IL}	Input low voltage		0		0.8	V

6.4 AC Electrical Characteristics (VCC = 20V, Ta = -20 ~ +105°C, unless specified)

Internal Oscillator

Parameter		Condition	Min.	Typ.	Max.	Units
f_{OSC}	Main oscillator frequency		9.5	10	10.5	MHz
f_{LFOSC}	Low frequency oscillator frequency		50	60	70	kHz

BMC Transmitter and Receiver

Parameter		Condition	Min.	Typ.	Max.	Units
f_{BMC}	BMC signal bit rate		270	300	330	kHz
t_{RISE_BMC}	BMC signal Tx rise time		300			ns
t_{FALL_BMC}	BMC signal Tx fall time		300			ns
t_{HOLD_BMC}	Time to cease driving the line after the final high-to-low transition		1			µs
t_{IFG_BMC}	Time from the end of last bit of a Frame until the start of the first bit of the next Preamble		25			µs
t_{END_BMC}	Time to cease driving the line after the end of the last bit of the Frame				23	µs
t_{RXFTR_BMC}	BMC receiver bandwidth limiting filter		100			ns
t_{NILDLE_BMC}	Time window for detecting non-idle		12		20	µs
N_{NIDLE_BMC}	Number of transitions to be detected to declare bus non-idle		3			

6.5 Thermal Resistance Notice

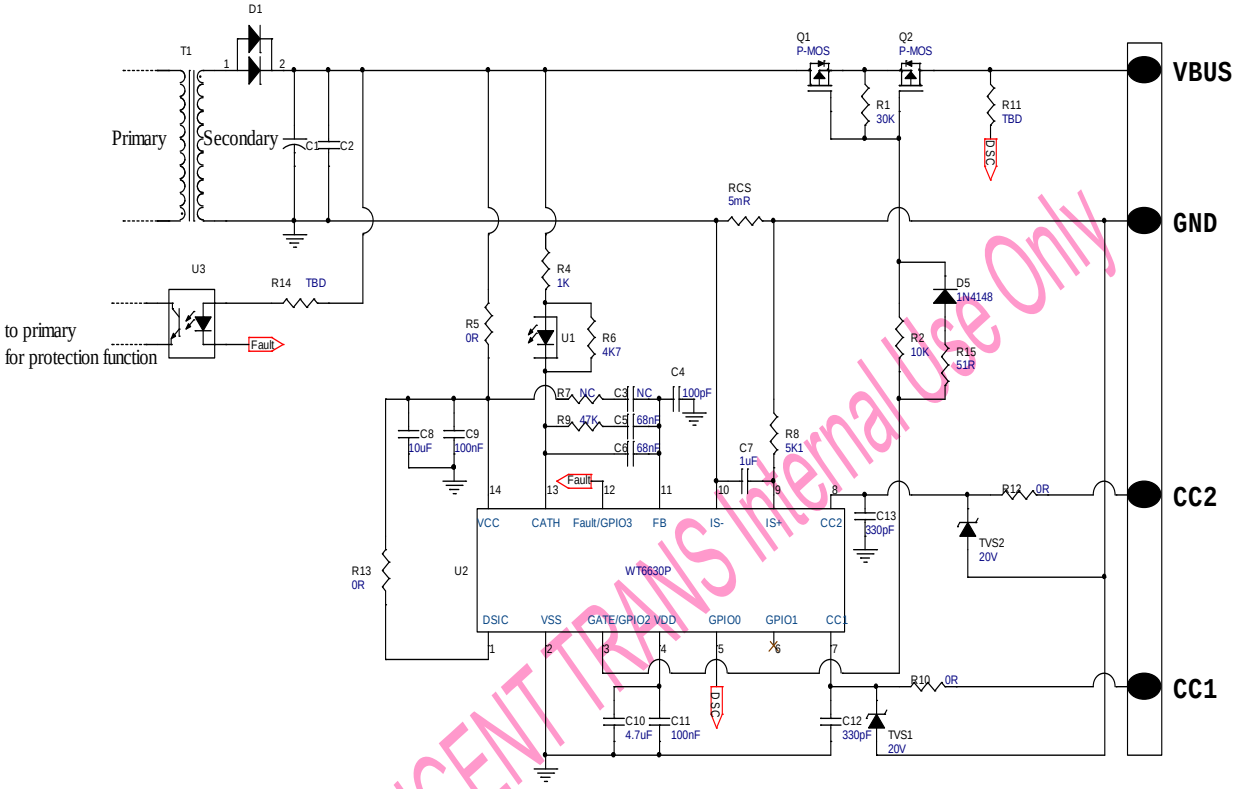
14-pin SOP

Parameter		Condition	Min.	Typ.	Max.	Units
θ_{JA}	Thermal Resistance (Junction to Air)			90		℃/W
θ_{JC}	Thermal Resistance (Junction to Case)			37		℃/W

16-pin QFN

Parameter		Condition	Min.	Typ.	Max.	Units
θ_{JA}	Thermal Resistance (Junction to Air)			2.6		℃/W
θ_{JC}	Thermal Resistance (Junction to Case)			37		℃/W

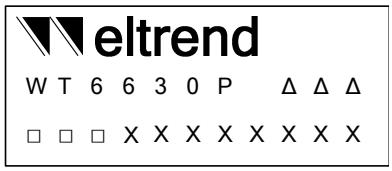
7. Example of Application Circuit



8. Ordering Information

Package Type	Package Outline	Part Number	Ordering Number	Transport Media
16-pin QFN	4mm x 4mm	WT6630P	WT6630P-UG160WT	Tray/Tapping
14-pin SOP	150 mil	WT6630P	WT6630P-SG140WT	Tube/Tapping

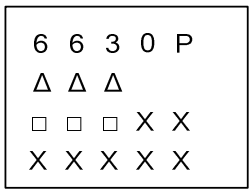
14-pin SOP top Mark



ΔΔΔ ROM Code

□□□ Date Code

16-pin QFN top Mark



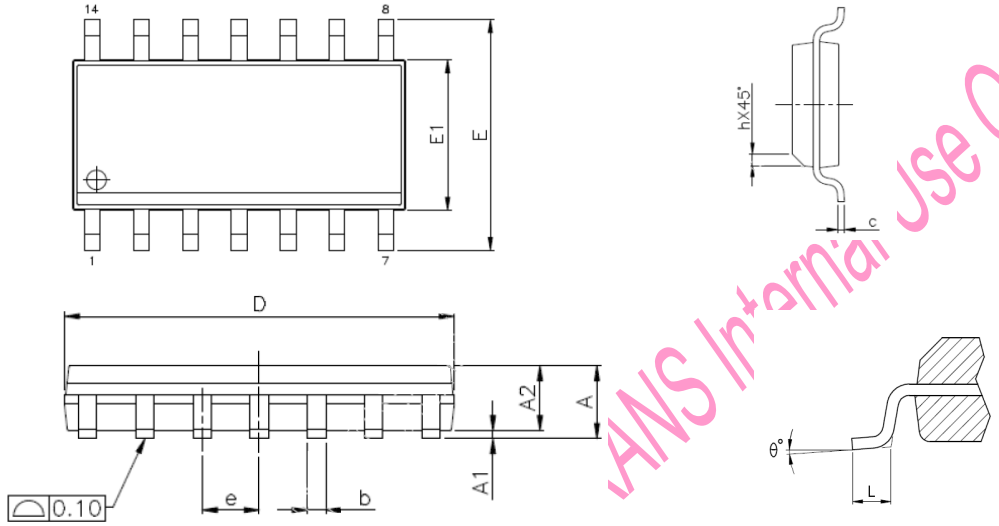
ΔΔΔ ROM Code

□□□ Date Code

9. Package Information

9.1 Package Dimensions

14-PIN SOP



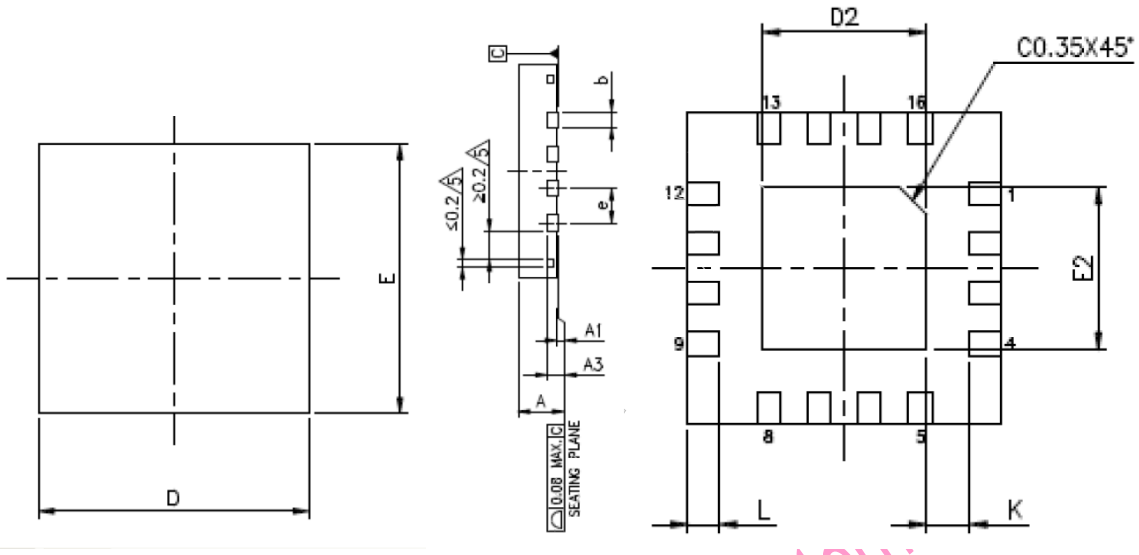
All dimensions shown in mm

SYMBOL	MIN.	MAX.
A	-	1.75
A1	0.10	0.25
A2	1.25	-
b	0.31	0.51
c	0.10	0.25
D	8.53	8.74
E	6.00 BSC	
E1	3.81	3.99
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

NOTES :

1. Dimensions “D” does not include mold flash, protrusions or gate burrs mold flash. Protrusions or gate burrs shall not exceed 0.15mm.
2. Dimensions “E1” does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed 0.25mm per side.

16-PIN QFN



All dimensions shown in mm

SYMBOL	MIN	NOR	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D		4.00	
E		4.00	
e		0.65	
K	0.20	-	-
L	0.35	-	0.50
D2	2.00	-	2.80
E2	2.00	-	2.80

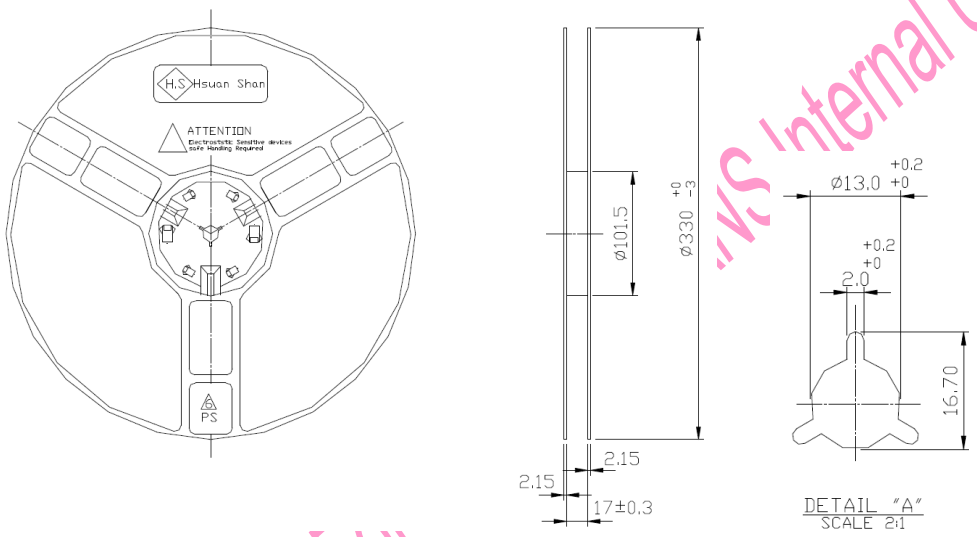
NOTE: Dimension “b” applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension “b” should not be measured in that radius area.

9.2 Product Tube and Tapping Specification

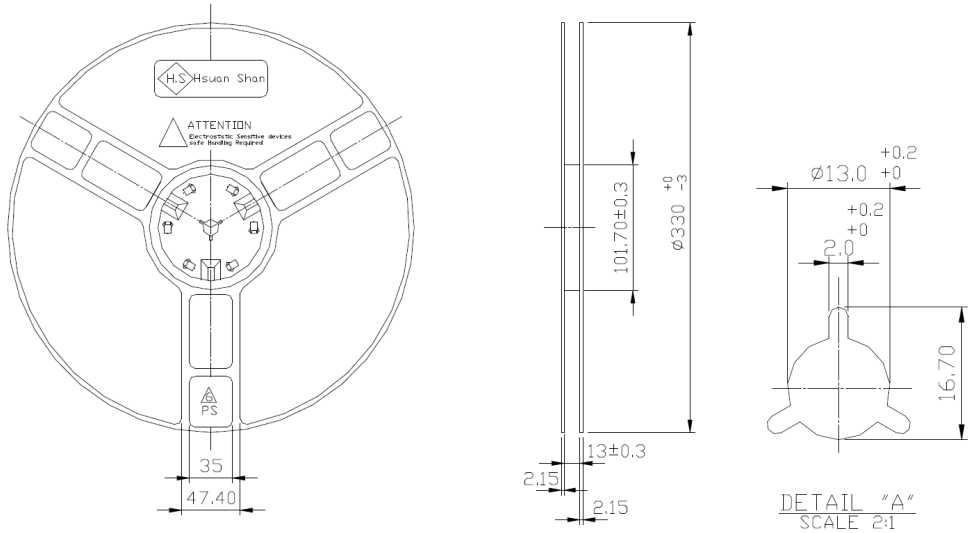
Package Type	EA/TUBE	TUBE/BOX	EA/BOX	Tapping (EA/Reel)
14-pin SOP (150 MIL)	58	300	17400	3000

Package Type	EA/TRAY	TRAY/BOX	EA/BOX	Tapping (EA/Reel)
16-pin QFN (4x4mm)	490	10	4900	2500

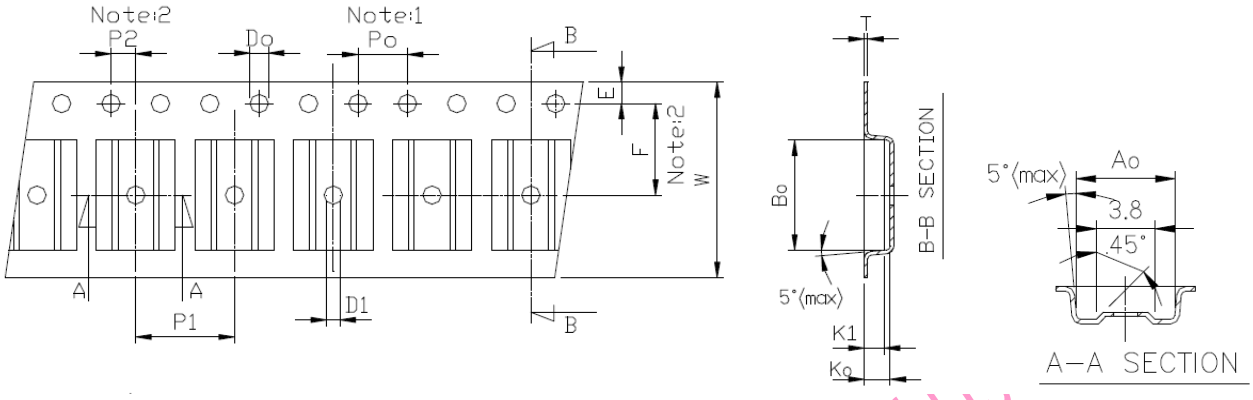
Reel Dimensions – 14pin SOP (W=16mm)



Reel Dimensions – 16pin QFN (W=12mm)



Carrier Tape Dimensions



Notes:

1. 10 Sprocket hole pitch cumulative tolerance is ±0.1mm
2. Pocket position relative to sprocket hole measured as true position of packet not pocket hole.
3. A_O and B_O measured on a plane 0.3mm above the bottom of the pocket to the top surface of the carrier.
4. K_O measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. Carrier camber shall be not than 1mm per 100 mm through a length of 250 mm.

Unit: mm

Symbol	14-Pin SOP	16-Pin QFN
A_O	6.40 ± 0.10	4.25 ± 0.10
B_O	9.00 ± 0.10	4.25 ± 0.10
K_O	2.12 ± 0.10	1.25 ± 0.10
K1	1.65 ± 0.10	-
P_O	4.00 ± 0.10	4.00 ± 0.10
P1	8.00 ± 0.10	8.00 ± 0.10
P2	2.00 ± 0.10	2.00 ± 0.05
D_O	1.50 ± 0.10	1.55 ± 0.05
D1	1.50 ± 0.10	1.50 (MIN)
E	1.75 ± 0.10	1.75 ± 0.10
F	7.50 ± 0.10	5.50 ± 0.05
$10P_O$	40.0 ± 0.10	40.0 ± 0.10
W	16.0 ± 0.30	12.0 ± 0.20
T	0.30 ± 0.10	0.30 ± 0.05

10. Revision History

Version	History	Date
1.0	Initial issue	May, 2015
1.05	Revision, see Errata for more details	June, 2015

Appendix: Errata

V1.0 -> V1.05

Item	Page	Chapter	Modification
1	4	4.1	Pin description content
2	5	5.1	Shunt regulator content
3	10	6.3	Electric Characteristics content
4	13	7	Update application circuit
5	14	8	Update ordering information - top mark