High Efficiency 8A Synchronous Buck Converter

Features

- **Ultra-High Efficiency**
- **Low Quiescent Current of 40μA**
- **Integrated 15mΩ at V5V=5V N-Channel MOSFET for Low Side**
- **Integrated 30mΩ at V5V=5V N-Channel MOSFET for High Side**
- **No Current-Sense Resistor (Lossless I_{LIMIT})**
- **Quasi-PWM with 100ns Load-Step Response**
- **1% VOUT Accuracy Over Line and Load**
- **Programmable Switching Frequency**
- **0.8V to 5.5V Adjustable Output Range**
- **4.5V to 26V Adapter or Battery Input Range**
- **Integrated Boost Switch**
- **UVP (non-latch)**
- **Over Temperature Protection (non-latch)**
- **3.3ms Soft-Start**
- **Power-Good Indicator**
- **Fixed 5V, 10mA Linear Regulator**

General Description

G5329 is a 8A, synchronous DC/DC buck converter with integrated 30mΩ N-channel high-side MOSFET and 15mΩ N-channel low-side MOSFET. It uses constant on-time control scheme to handle wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency. The G5329 achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Single-stage buck conversion allows these devices to directly step down high-voltage batteries for the highest possible efficiency. The built-in 5V LDO supports 10mA for internal circuit. The G5329 is intended for the main power supply for the networking system or other low-voltage supplies as low as 0.8V. The G5329 is available in QFN4X4-32 package.

Applications

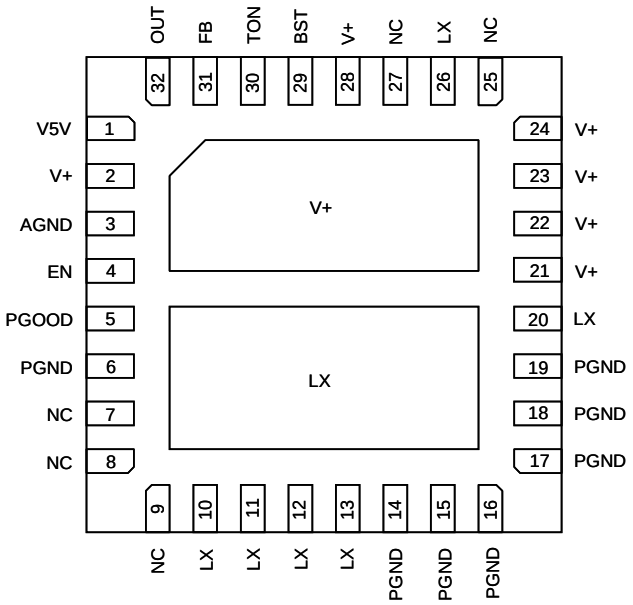
- **I/O Supply**
- **Networking Power Supply**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G5329QV1U	5329	-40°C to +85°C	QFN4X4-32

Note: QV: QFN4X4-32
1: Bonding Code
U: Tape & Reel
Green: Lead Free / Halogen Free

Pin Configuration



G5329 QFN4X4-32

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Absolute Maximum Ratings

V+ to AGND . . . . . -0.3V to 30V
V5V to AGND . . . . . -0.3V to 6V
PGOOD, OUT, EN to AGND . . . . . .-0.3V to 6V
FB, TON to AGND . . . . . .-0.3V to (V5V+0.3V)
BST to PGND . . . . . .-0.3V to 35V
LX to BST . . . . . -6V to 0.3V

Thermal Resistance of Junction to Ambient (θ_{JA})
QFN4X4-32 . . . . . 25°C/W
Junction Temperature . . . . . .150°C
Storage Temperature . . . . . -65°C to 150°C
Reflow Temperature (soldering, 10sec) . . . . . 260°C

Electrical Characteristics

(VIN=12V, V5V=5V, EN=5V, T_A=25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V+ Input Voltage Range	V+	4.5	---	26	V
LDO Output Voltage	V5V	4.75	5.0	5.25	V
Line Regulation of V5V	Load=1mA; V+=8V to 26V	---	5	30	mV
Load Regulation of V5V	Load=10mA	---	---	70	mV
Dropout Voltage of V5V	Load=10mA	---	1.0	1.2	V
Error Comparator Threshold (DC Output Voltage Accuracy)	V+=12V, FB=OUT	788	800	812	mV
Soft-Start Ramp Time	Rising edge of EN to 95% output voltage	---	3.3	---	ms
TON Operating Current	R_{TON} = 240kΩ, V+=12V	---	50	---	µA
On Time	V+=12V, VOUT=3.3V, R_{TON}=240kΩ, nominal	---	660	---	ns
Minimum On Time	VOUT=0.1V, R_{TON}=240kΩ	---	80	---	ns
Minimum Off Time	FB=0.7V, LX=-0.1V,	---	300	---	ns
Quiescent Supply Current (V+)	FB forced above the regulation point	---	40	---	µA
Shutdown Current (V+)		---	1	---	µA
Output Shutdown Discharge Resistance	EN=AGND	---	12	32	Ω
Output Undervoltage Protection Threshold	With respect to error comparator threshold	60	70	80	%
Output Undervoltage Protection Blanking Time	From EN signal going high	---	3	---	ms
Current-Limit Threshold		8	---	---	A
Zero Current Threshold (Zero Crossing)	PGND - LX	---	3	---	mV
PGOOD Trip Threshold	Measure at FB with respect to error comparator threshold, falling edge. Hysteresis=32mV	-14	-10	-7.5	%
PGOOD Output Low Voltage	ISINK=1mA	---	---	0.2	V
PGOOD Propagation Delay		---	5	16	µs
Thermal Shutdown Threshold	Hysteresis=20°C	---	165	---	°C
V5V Undervoltage Lockout Threshold	Rising edge, hysteresis = 200mV,PWM disabled below this level	3.7	---	4.3	V
High Side Switch Resistance	BST - LX forced to 5V, V5V=5V	---	30	40	mΩ
Low Side Switch Resistance	V5V=5V	---	15	20	mΩ
BST Switch Forward Voltage	Forwarding Current=10mA	0.2	0.35	0.4	V
Logic Input High Voltage	EN	1.4	---	V5V	V
Logic Input Low Voltage	EN	---	---	0.7	V

Pin Description

PIN	NAME	FUNCTION
1	V5V	5V Linear Regulator Output. Supply for Internal circuits. Bypass to AGND with a 10µF (min) ceramic capacitor.
2, 21, 22, 23, 24, 28	V+	Power Supply Input. V+ is used to set the PWM one-shot Timing. Bypass to GND with a 4.7µF (min) Capacitor.
3	AGND	Analog Ground
4	EN	Enable Input. Enable the 5V LDO and Buck Converter.
5	PGOOD	Power-Good Open-Drain Output. PGOOD is low when the output voltage is more than 10% below the normal regulation point or during soft-start. PGOOD is high impedance when the output is in regulation and the soft-start circuit has terminated.
6, 14,15,16, 17, 18, 19	PGND	Power Ground. Source node of low side power MOSFET.
7, 8, 9, 25, 27	NC	No connection
10, 11, 12, 13, 20, 26	LX	External Inductor Connection. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver. LX is also the positive input to the current-limit comparator.
29	BST	Boost Flying-Capacitor Connection. Connect to an external capacitor according to the Standard Application Circuit. See *MOSFET Gate Drivers (DH, DL)* section.
30	TON	On-Time Selection-Control Input. Connect to LX with a resistor, R_{TON}.
31	FB	Feedback Input. Connect FB to a resistor divider from OUT for an adjustable output.
32	OUT	Output Voltage Connection. Connect directly to the junction of the external and output filter capacitors. OUT senses the output voltage to determine the on-time.

Block Diagram

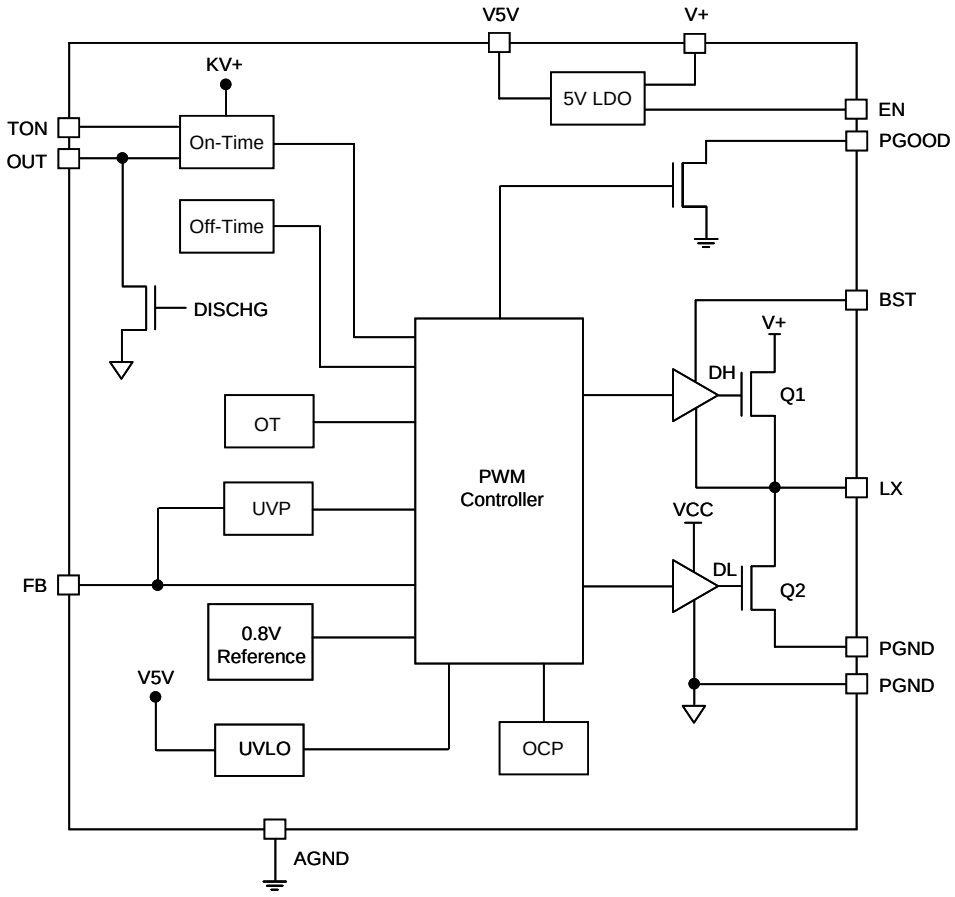


Fig. 1 Block Diagram of G5329

Application Information

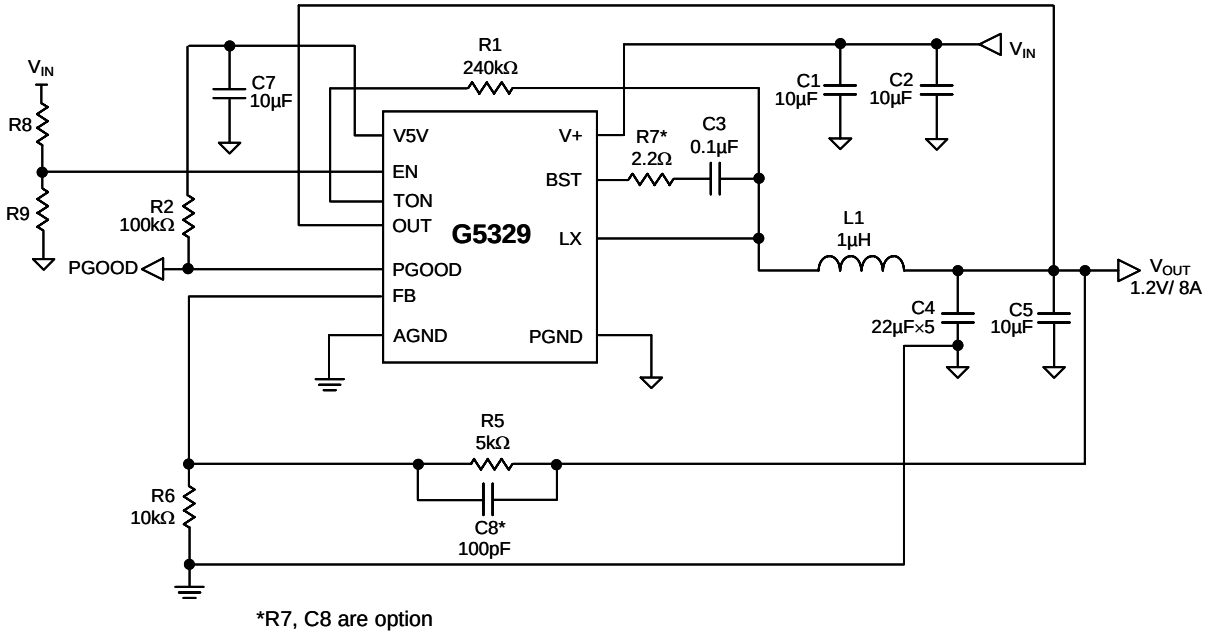


Fig. 2-A Standard Application Circuit

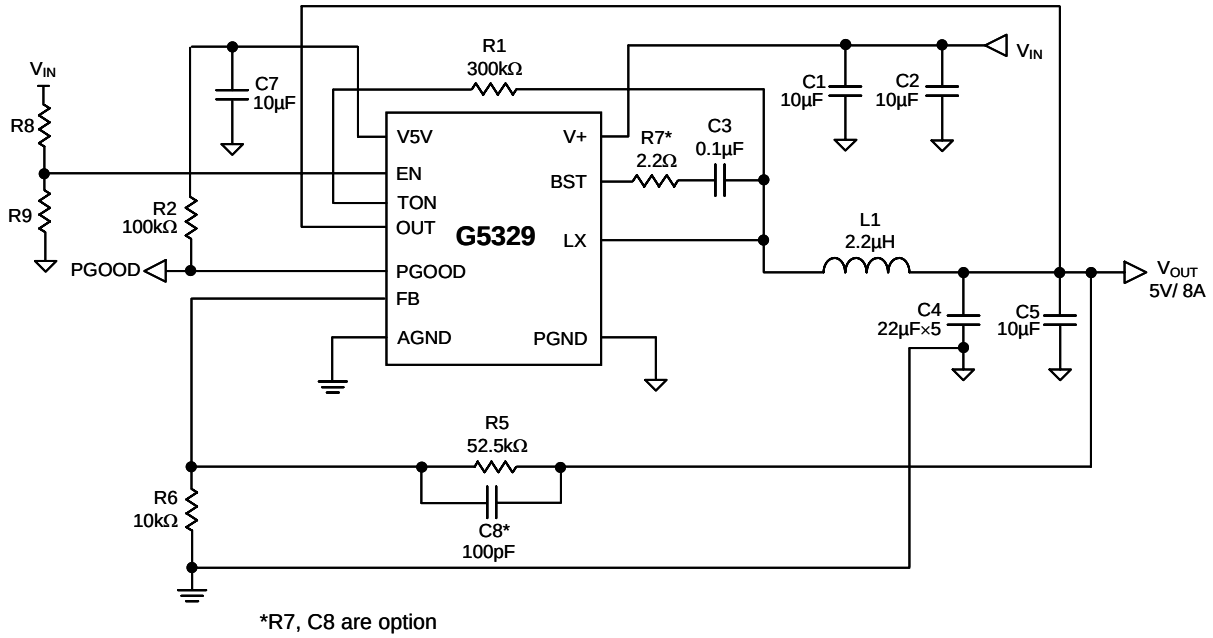


Fig. 2-B Standard Application Circuit

Detailed Description

G5329 is a 8A, synchronous buck converter with a fixed 5V LDO. A Quasi-PWM control is adapted in G5329. It is a constant-on-time PWM control with input feed-forward while maintaining a relatively constant switching frequency. It advantages in the fast load-transient response compared with conventional constant-on-time PWM control. The Figure 2 shows the Block Diagram of G5329. An EN pin is provided to turn on/off G5329. It is recommended to connect a resistor divider from V+, or controlled by enable signal no more than 5.5V.

5V Linear Regulation

G5329 contains a LDO with fixed 5V output (V5V) enable by EN. It supports up to 10mA for the internal PWM circuit and gate-drivers. It can not support external circuit. Bypass V5V to AGND with 10µF (min) capacitor and close to the device.

Constant-on-time PMW Control with Input Feed-Forward

The Quasi-PWM control algorithm can be described briefly: the high-side switch on-time is determined by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another on-shot determines the minimum off-time. The on-time one-shot can be triggered if the error comparator is low, the low side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time Selection

G5329 allows to program the on-time. The on time is determined as below

$$T_{ON} = \frac{R_{TON} \times V_{OUT}}{(V_{IN} - 0.8)} \times 9.33 \times 10^{-12} \qquad (V_{OUT} < 4V)$$

$$T_{ON} = \frac{R_{TON}}{(V_{IN} - 0.8)} \times 3.73 \times 10^{-11} \qquad (V_{OUT} \geq 4V)$$

It results in a nearly constant switching frequency R_{TON} is a resistor connected from LX to the TON pin.

Pulse-Skipping Mode

In Pulse-Skipping Mode, an automatic switchover to PFM takes place at light load. It turns off the low side switch when the inductor current crosses to zero. This scheme will improve the light-load efficiency.

Current Limit

G5329 uses the on-state resistance of low side MOSFET as a current-sensing resistor. If the current–sense voltage (PGND-LX) is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is the current-limit threshold adding one inductor current ripple. So it depends on the on-resistance of MOSFET, Inductor value, and battery voltage. No external current-sensing resistor is necessary in the output current path. The current limit threshold is set above 8A internally.

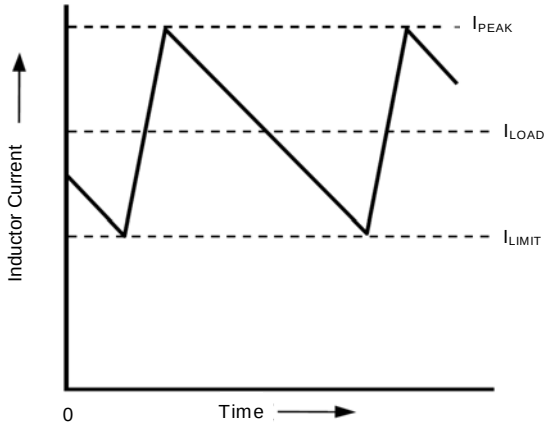


Fig. 3 Current Limit Setting

Gate Drivers

In the low duty factor application, it exists large difference of input voltage and output voltage. Therefore, large low-side MOSFET and moderate-size high-side MOSFET are needed for high efficiency. The DH and DL drivers are optimized for driving high-side and low-side MOSFETs. A non-overlap control circuit is needed to avoid the DH and DL turning on simultaneously. The DL driver with a 0.5Ω pull low transistor helps prevent the DL from being coupled to high during the fast rising-time of the LX node, due to the drain to gate capacitive coupling of low-side synchronous-rectifier MOSFET. A resistor in series with the BST is recommended that will reduce the EMI-producing efficiency loss by increasing the turn-on time of the high-side MOSFET.

UVLO and Soft-Start

When V5V is below 4V, undervoltage lockout (UVLO) inhibits switching and forces DL to high. It reset the fault latch and soft-start counter. An internal soft-start timer ramps up the current limit threshold to 100% of current limit setting within 3.3ms.

Power-Good Indicator

The Output voltage is always monitored for undervoltage by the PGOOD comparator. The PGOOD is open-drain type signal. In shutdown and soft-start period, PGOOD is kept low. After the soft-start timer has timed out, the PGOOD could be activated. A CD pin could be adjusted the PGOOD propagation delay time if the output voltage is within 10% of normal value.

Fault Protection

G5329 provides undervoltage protection, overvoltage protection, and overtemperature protection.

The undervoltage protection (UVP) function is like foldback current limit function. If the output voltage is under 70% of normal value 3ms after shutdown released, the undervoltage protection function is activated. The SMPS would turn off high-side and low-side MOSFETS, and restart after 9ms.

The G5329 has an overtemperature protection (OTP) that occurs when the die temperature is above 165°C. It will shutdown the SMPS and force high-side and low-side gate drivers output low. It could be released when die cool down or EN is toggled.

Adjustable-Output Feedback

Connecting the FB pin to a resistor divider between OUT to GND to adjust the output voltage between 0.8V to 5.5.V.

Chose R6=10kΩ and solve the R5 with the equation:

$$R5 = R6 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V_{FB} = 0.8V norminal.

Application Information

Inductor Selection

The inductor value is determined as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f \times \Delta I_{LPP}}$$

Where ΔI_{LPP} is defined as inductor ripple current.

The inductor ripple current also impacts transient-response performance, especially at low V_{IN}- V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step.

Maintaining the ratio of the inductor ripple current to the designed maximum load current within a 20% to 50% range is prudent.

Output Capacitor Selection

The output filter capacitor could be used with MLCC type capacitor. It is recommended to use 22µFx5 (minimum) as output capacitor for 500kHz switching frequency application.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-upsurge currents.

For optimal circuit reliability, choose a capacitor that has less than 10°C temperature rise at the peak ripple current.

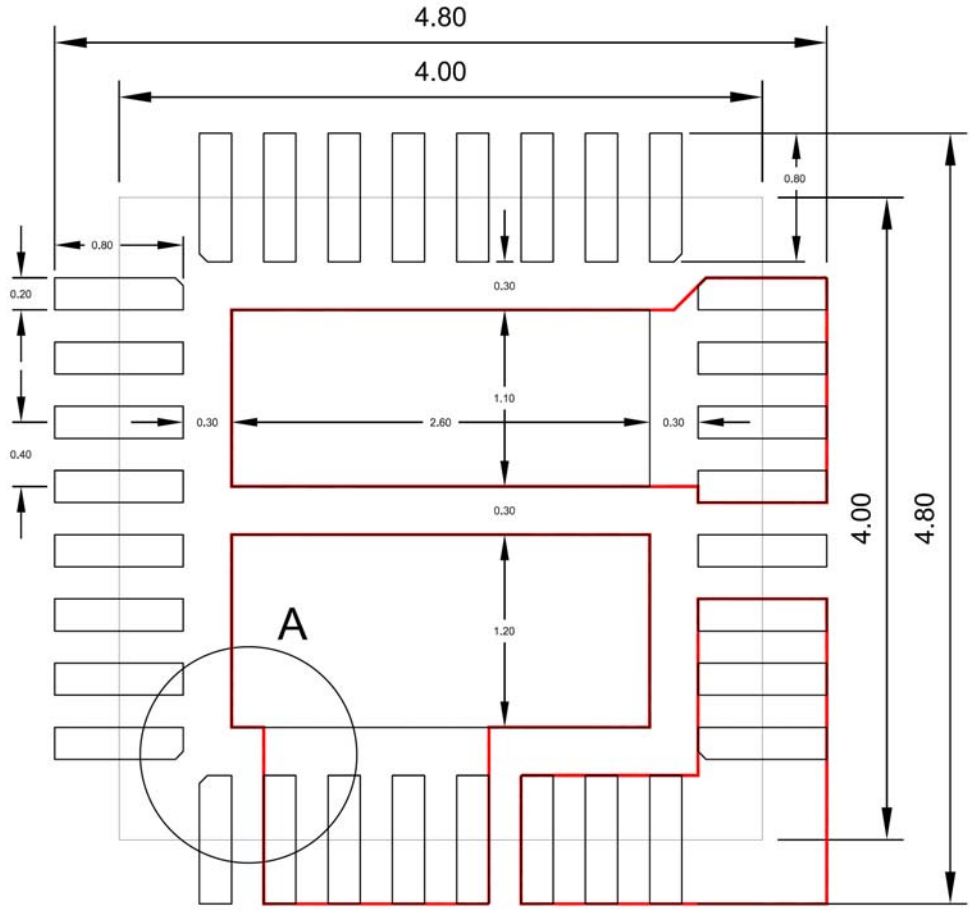
$$I_{RMS} = I_{LOAD}\left(\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}\right)$$

Layout Considerations

- Connect AGND (Pin3) to ground of bypass V5V and FB path.
- Connect AGND and PGND together close to the IC and the negative terminal of C_{OUT}.
- Star connection PGND ground plane to system ground (normally, it's defined as ground of power supply or battery pack.).
- Connect PGND of power component Low-side MOSFET source, C_{IN}, and C_{OUT} to system ground by a plane.
- All sensitive analog traces such as OUT, and FB should be placed away from high-voltage switching node such as LX, BST nodes to avoid coupling.

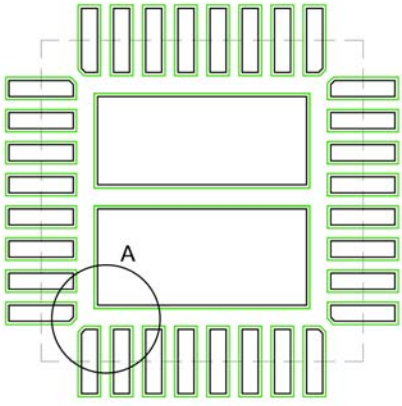
Minimum Footprint PCB Layout Section

QFN4X4-32

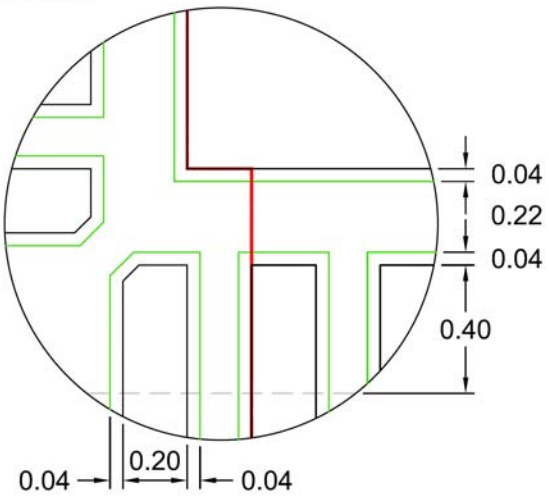


Top Layer

* Recommend Top Layer Thermal Pad Design Following Red Line for Better Characteristic.

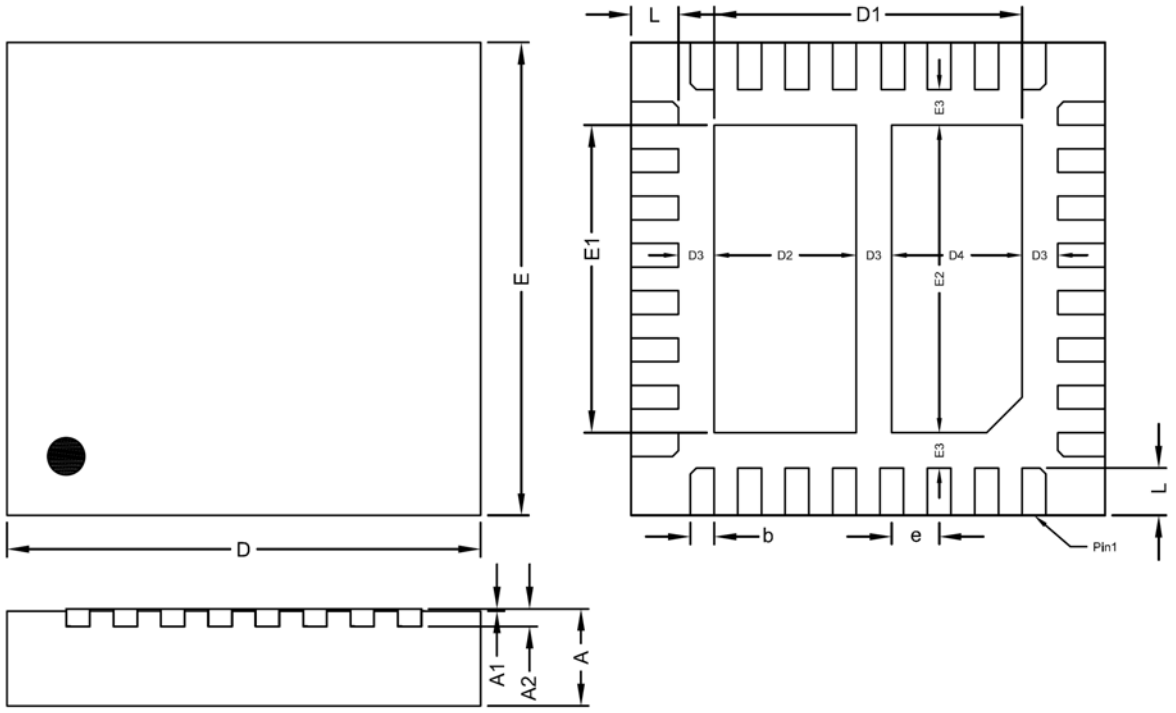


Top Layer with Solder Mask



Section A

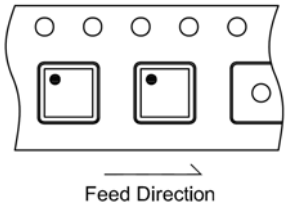
Package Information



QFN4X4-32 Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.0276	0.0315	0.0354
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2		0.20 BSC			0.0079 BSC	
D	3.95	4.00	4.05	0.1555	0.1575	0.1594
E	3.95	4.00	4.05	0.1555	0.1575	0.1594
D1	2.50	2.60	2.70	0.0984	0.1023	0.1063
E1	2.50	2.60	2.70	0.0984	0.1023	0.1063
D2	1.15	1.20	1.25	0.0453	0.0472	0.0492
E2	2.55	2.60	2.65	0.1004	0.1024	0.1043
D3		0.30 BSC			0.0118 BSC	
E3		0.30 BSC			0.0118 BSC	
D4	1.05	1.10	1.15	0.0413	0.0433	0.0453
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e		0.40 BSC			0.0157 BSC	
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/BY REEL
QFN4X4-32	3,000 ea

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