Alpha Analog Technology, Inc.

AAP6150A

7.5V to 40V Input Supply, Synchronous Buck PWM Controller

FEATURES

- **Wide 7.5V to 40V Input Voltage Range**
- **Drive Dual Low Cost N-Channel MOSFETs -Adaptive Shoot-Through-Protection**
- **High Efficiency Up to 93% at 5A**
- **0.8V reference with +/- 1.5% accuracy**
- **Fast Load Transient Response**
- **Dual Output with Independent Programmable Over-Current Control**
- **Over-Current Control Accuracy +/-3%**
- **Nearly Zero Input Current at Output Over Current Protection or Output Under- Voltage Protection**
- **Internal Soft-Start**
- **Programmable Output Cable Compensation**
- **200kHz Fixed Switching Frequency**
- **Thermal shutdown Protection**
- **Available in MSOP-10 Package**
- **RoHS Compliant and Halogen Free**

APPLICATIONS

- Car Charger/Adaptor
- Rechargeable Portable Devices
- Battery Charger

DESCRIPTION

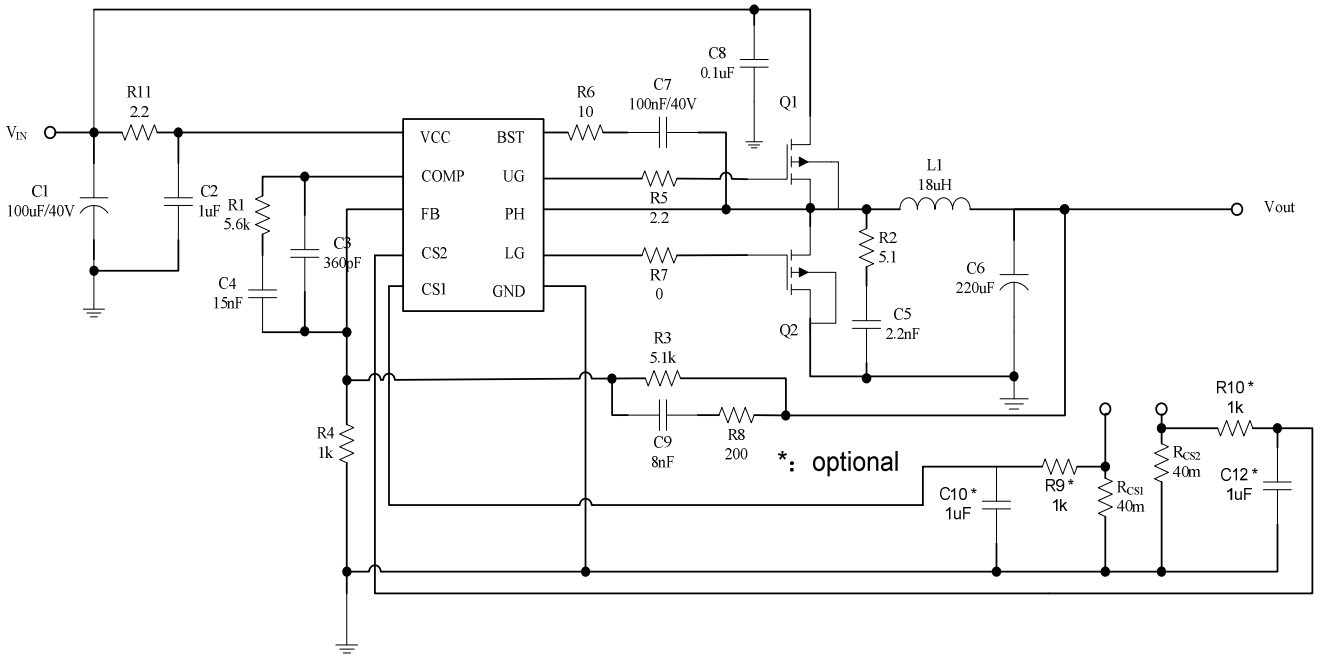
The AAP6150A is a voltage mode synchronous buck controller that achieves excellent load and line regulation. The device operates from an input voltage range of 7.5V to 40V.The AAP6150A provides protection functions including: input under-voltage lockout, output under-voltage protection and programmable over-current protection with two independent outputs.

The AAP6150A is housed in a MSOP10 Package.

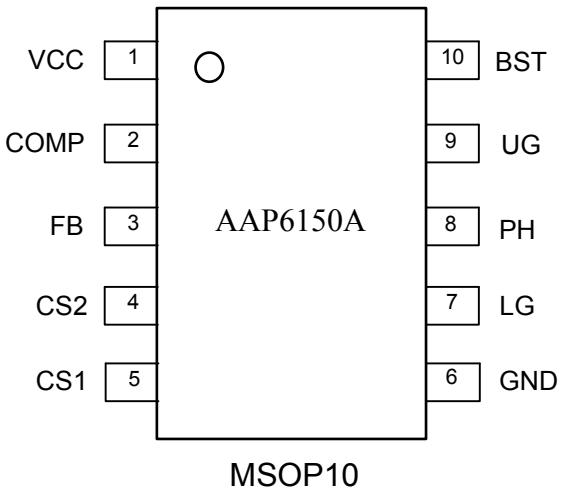
ORDERING INFORMATION

Order Information	Top Marking
AAP6150 A SA 10 Extension Code Package Type ES: MSOP-10 Pin Count	AAP6150A → Part Number X J X X X X — Day Month Year Wafer version code Assembly house code Production code

TYPICAL APPLICATION



PIN CONFIGURATION



MSOP10

ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

VCC .....–0.3V to 40V

PHASE(DC) .....–1.0V to (VCC+1)V

UG .....V_{PHASE}–0.3V to V_{BST}+0.3V

BST.....(V_{PHASE}-0.3)V to (V_{PHASE}+7)V

FB, COMP, CS1, CS2, LG ..... –0.3V to 7V

Operating Temperature Range .....–40°C to 150°C

Storage Temperature Range .....–55°C to 150°C

ESD Rating

HBM (Human Body Mode) 2KV

MM (Machine Mode) 200V

PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	VCC	Supply Input
2	COMP	Output pin of error amplifier, Connect an appropriate compensation network between this and the FB pin
3	FB	Output Voltage Feedback Input.
4	CS2	Vout2 Output Over-Current Detection Pin. When this pin sense the voltage drop of sense-resistor RCS2 greater than 120mV for 30µs, the IC shut down for about 1.3 seconds before restart.
5	CS1	Vout1 Output Over-Current Detection Pin. When this pin sense the voltage drop of sense-resistor RCS1 greater than 120mV for 30µs, the IC shut down for about 1.3 seconds before restart.
6	GND	Ground. Connect this pin to the PCB ground
7	LG	Output to external low-side gate driver
8	PHASE	Switching node： Connect this pin to the drain of low-side MOSFET and the source of hide-side MOSFET.
9	UG	Output to external high-side gate driver
10	BST	Bootstrap pin. Connect a 100nF capacitor for BST pin to PHASE pin. This capacitor provides power supply to the integrated high-side MOSFET gate driver.

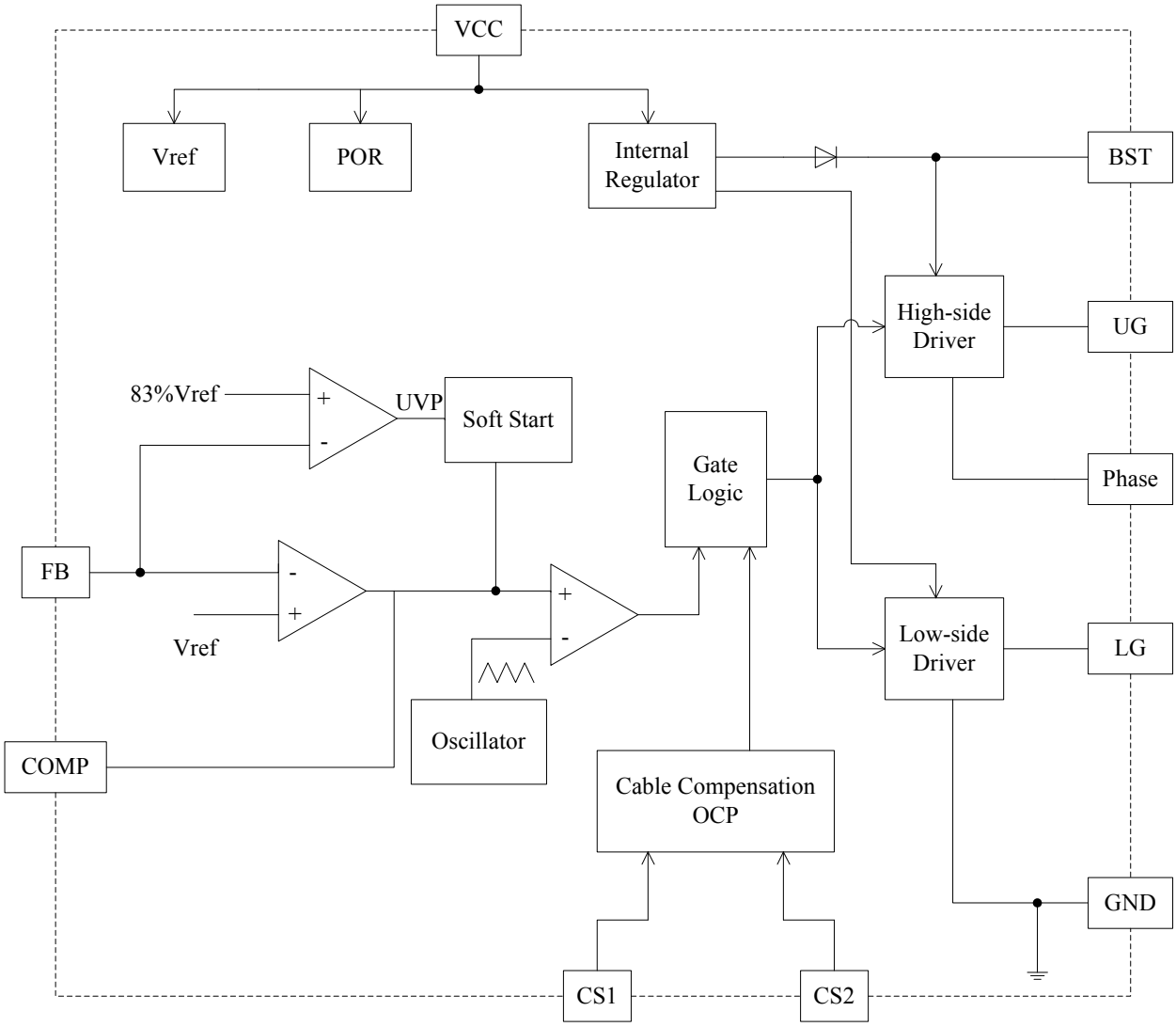
Note: Connect the exposed pad of the package to a large ground copper area for maximum heat dissipation.

ELECTRICAL CHACRACTERISTICS

(V_{CC} = 12V, unless otherwise specified. Typical values are at TA = 25°C.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Input						
Supply voltage range	V_{CC}		7.5		40	V
Supply input current	I_{CC}	V_{FB}=0.7V		2.8		mA
Power-On Reset						
Rising VCC threshold				7.0		V
Falling VCC threshold				6.1		V
Oscillator and Soft-Start						
Switching Frequency	F_{OSC}			200		kHz
Sawtooth Amplitude	ΔV_{OSC}			1.6		V
Soft-Start Time	T_{SS}			2		mS
Reference Voltage						
Reference Voltage	V_{REF}	Measured at FB Pin		0.8		V
Accuracy		T_A=-20~80°C	-1.5		+1.5	%
PWM Controller Gate Drivers						
UGATE Maximum Voltage		V_{UG}-V_{PHASE}		5.5		V
LGATE Maximum Volatge		V_{LG}-V_{GND}		5.5		V
UGATE Source Output Impedance	$R_{DS(ON)}$	IGATE=100mA		4.3		Ω
UGATE Sink Output Impedance	$R_{DS(ON)}$	IGATE=100mA		3.4		Ω
LGATE Source Output Impedance	$R_{DS(ON)}$	IGATE=100mA		3.6		Ω
LGATE Sink Output Impedance	$R_{DS(ON)}$	IGATE=100mA		1.3		Ω
Over current Protection and FB Under Voltage Protection						
CS1 OCP threshold	V_{CS1}		116.5	120	123.5	mV
CS2 OCP threshold	V_{CS2}		116.5	120	123.5	mV
OCP Debounce Time	T_{OCP}			30		µS
FB Under Voltage Threshold	V_{FB-UV}	Percent of V_{REF}		83		%
Recycle Time	T_R	FB UV or OCP		1.3		S

BLOCK DIAGRAM



DETAIL DESCRIPTION

The AAP6150A is a synchronous voltage-mode buck PWM controller with programmable dual-output over-current control.

Initialization

The AAP6150A creates its own internal supplies for use. The POR function continually monitors the input bias supply voltage at the VCC pin. The POR function initiates soft-start operation after VCC supply voltages exceed its POR rising threshold voltage.

Soft-start

The AAP6150A has an internal soft-start circuitry to reduce supply inrush current during startup conditions. The typical soft-start time is about 2ms. The Power-On-Reset function initiates the soft-start process. Once the VCC voltage falls below 6.1V, the controller will shut down until the voltage exceeds 7V again.

Switch Frequency

The on-chip oscillator clock switches at 200kHz

normally.

Over-Current and UVP Protection

When the load current is less than the current-limit, the AAP6150A will regulate the output voltage and operates in the constant voltage mode. If the load current increased beyond the current-limit sensed by the CS1 pin or CS2 pin and this over-current condition is continuous for 30μs , then the AAP6150A will stop switching for about 1.3 seconds before initiating a new soft start, if the over current condition is not removed, the converter will hiccup. During this long time sleeping at over-current or output under-voltage condition, the input current of the system is nearly zero.

OVP and Thermal Shutdown

If the output voltage is higher than regulation target the AAP6150A will immediately stop switching the high-side MOSFET but not low-side MOSFET. The AAP6150A will not open the high-side MOSFET until the output voltage decrease to regulation target.

Over temperature protection limits total power dissipation in the device. When the junction temperature exceeds TJ= +150°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 15°C.

BST Capacitor, Bootstrap Refresh

A capacitor from the PHASE pin to the BST pin is required for the bootstrap circuit for the High-side Gate driver. The voltage of the PHASE pin can go as high as the supply voltage during the Hside-MOSFET opens. A diode is included on the IC (anode to internal PVCC, cathode to BST pin), such that the PVCC will be the bootstrap supply. In the event that the UGATE is on for an extended period of time, the charge on the BST capacitor can start to sag, raising the $R_{DS(ON)}$ of the Hside-MOSFET. The AAP6150A has a circuit that detects a long UGATE on-time (7.5 oscillator clock periods), and forces the LG to go high for half an oscillator cycle, which allows the bootstrap capacitor to recharge.

DESIGN PROCEDURE

Setting Output Voltages

Output voltages are set by external resistors. The V_{REF} is 0.8V. According to the typical application diagram:

$$V_{OUT} = V_{REF}\left(1 + \frac{R_1}{R_2}\right)$$

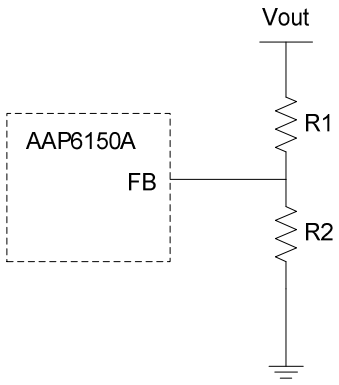


FIGURE 1. Setting VOUT with a Resistor-Divider

Setting Over-Current Threshold

The output over-current value is set by a sense resistor between CSx (x=1 or 2) pin and GND, according to the following equation:

$$I_{OCP} = \frac{120mV}{R_{CS}}$$

Output Cable Compensation

Output cable compensation voltage can be set by R1 (FIGURE 1). The relationship between R1 and output cable compensation voltage is calculated below:

If $V_{CS1} \geq V_{CS2}$,

$$\Delta V_{OUT1} = \frac{3 \cdot V_{CS1} \cdot R1}{10k\Omega} - V_{CS1}$$

$$\Delta V_{OUT2} = \frac{3 \cdot V_{CS1} \cdot R1}{10k\Omega} - V_{CS2}$$

If $V_{CS1} < V_{CS2}$,

$$\Delta V_{OUT1} = \frac{3 \cdot V_{CS2} \cdot R1}{10k\Omega} - V_{CS1}$$

$$\Delta V_{OUT2} = \frac{3 \cdot V_{CS2} \cdot R1}{10k\Omega} - V_{CS2}$$

Inductor Selection

The external components required for the step-down are an inductor, input and output filter capacitors, and compensation RC network. AAP6150A provides best efficiency with continuous inductor current. A reasonable inductor value (L_{IDEAL}) can be derived from the following:

$$L_{IDEAL} = \frac{V_{IN} D(1-D)}{f_{SW} I_{OUT} K_{RIPPLE}}$$

Where, K_{RIPPLE} is the ratio of the inductor peak-to-peak current to the inductor DC current, usually, we set K_{RIPPLE} between 20%-50%. D is the duty cycle:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Given L_{IDEAL}, the peak-to-peak inductor current is $K_{RIPPLE}I_{OUT}$. The absolute-peak inductor current is $I_{OUT}(1+0.5K_{RIPPLE})$. Inductance values smaller than L_{IDEAL} can be used to reduce inductor size; however, if much smaller values are used, inductor current rises, and a larger output capacitance may be required to suppress output ripple. Larger values than L_{IDEAL} can be used to obtain higher output current, but typically with larger inductor size.

Input Capacitor Selection

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during normal switching, its ESR also affects efficiency.

Use small ceramic capacitors (C_{HF}) for high frequency decoupling and bulk capacitors to supply the surge current needed each time high-side MOSFET turns on.

Place the small ceramic capacitors physically close to the MOSFETs and between the drain of high-side MOSFET and the source of low-side MOSFET.

The input buck capacitor should also be placed close to the upper-MOSFET's drain and GND, with the shortest layout traces possible. The important parameters for the buck input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline.

The RMS current is given by:

$$I_{RMS} = I_{OUT} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

I_{RMS} has a maximum at $V_{IN}=2V_{OUT}$, where $I_{RMS}=I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Output Capacitor Selection

The output capacitor is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response.

The output ripple is given by:

$$\Delta V_{OUT} \le \Delta I_L (R_{ESR} + \frac{1}{8F_{SW}C_{OUT}})$$

The output ripple will be highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement.

EMI Consideration

Since parasitic inductance and capacitance effects in PCB circuitry would cause a spike voltage on PHASE node when high-side MOSFET is turned on/off, this spike voltage on PHASE may impact on EMI performance in the system. In order to enhance EMI performance, there are two methods to suppress the spike voltage. One is to place an RC snubber between PHASE and GND and make them as close as possible to the high-side MOSFET's source and low-side MOSFET's drain. Another method is to add a resistor in series with the boostrap capacitor C1. But this method will decrease the driving capability to the high-side MOSFET. It is strongly recommended to reserve the RC snubber during PCB layout for EMI improvement. Moreover, reducing the PHASE trace area and keeping the main power in a small loop will be helpful on EMI performance.

Compensation

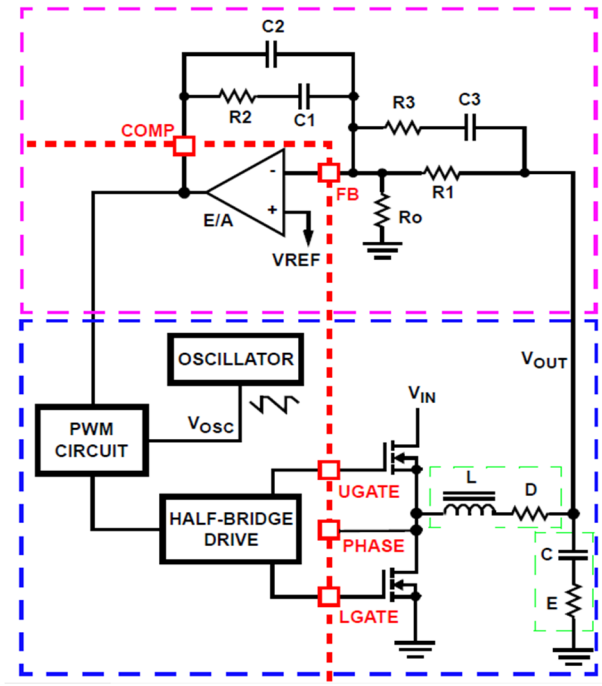


FIGURE 2. Voltage-Mode Buck Converter Compensation

Design

The AAP6150A uses voltage-mode control to achieve compensation and fast load transient response. A type-3 feedback network is recommended (see Figure 2).

The output voltage (V_{OUT}) is regulated by V_{REF}. The error amplifier output (COMP pin voltage) is compared with the oscillator (OSC) modified saw-tooth wave to provide a pulse-width modulated wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L and C). The output filter capacitor bank's equivalent series resistance is represented by the series resistor E.

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function is dominated by a DC gain, given by $D*V_{IN}/\Delta V_{OSC}$, and shaped by the output filter, with a double pole break frequency at F_{LC} and a zero at F_{CE}. For the purpose of this analysis, L and D represent the channel inductance and

its DCR, while C and E represent the total output capacitance and its equivalent series resistance.

$$F_{LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \qquad F_{CE} = \frac{1}{2 \cdot \pi \cdot C \cdot E}$$

The compensation network consists of the error amplifier (internal to the AAP6150A) and the external R1-R3, C1-C3 components. The goal of the compensation network is to provide a closed loop transfer function with high 0dB crossing frequency (F_0: typically 0.1 to 0.3 of F_{SW}) and adequate phase margin (better than 45 degrees). Phase margin is the difference between the closed loop phase at F_{0dB} and 180°.The equations that follow relate the compensation network's poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 2.

Use the following guidelines for locating the poles and zeros of the compensation network:

1. Select a value for R1 (1kΩ~10kΩ, typically). Calculate value for R2 for desired converter bandwidth (F_0). If setting the output voltage via an offset resistor connected to the FB pin, R_0 in Figure 2, the design procedure can be followed as presented.

$$R2 = \frac{\Delta V_{OSC} \cdot R1 \cdot F_0}{D \cdot V_{IN} \cdot F_{LC}}$$

2. Calculate C1 such that F_{Z1} is placed at fraction of the FLC, at 0.1 to 0.75 of F_{LC} (to adjust, change the 0.5 factor to desired number). The higher the quality factor of the output filter and/or the higher the ratio F_{CE}/F_{LC}, the lower the F_{Z1} frequency (to maximize phase boost at F_{LC})

$$C1 = \frac{1}{2\pi \cdot R2 \cdot 0.5 \cdot F_{LC}}$$

3. Calculate C2 such that F_{P1} is placed at F_{CE}.

$$C2 = \frac{C1}{2\pi \cdot R2 \cdot C1 \cdot F_{CE} - 1}$$

4. Calculate R3 such that F_{z2} is placed at F_{LC}. Calculate C3 such that F_{P2} is placed below F_{SW} (typically, 0.5 to 1.0 times F_{SW}). F_{SW} represents the switching frequency. Change the numerical factor to reflect desired placement of this pole. Placement of F_{P2} lower in frequency helps reduce the gain of the compensation network at high frequency, in turn reducing the HF ripple component at the COMP pin and minimizing resultant duty cycle jitter.

$$R3 = \frac{R1}{\frac{F_{SW}}{F_{LC}} - 1}$$

$$C3 = \frac{1}{2\pi \cdot R3 \cdot 0.7 \cdot F_{SW}}$$

APPLICAITION INFORMATION

Layout is critical to achieve clean and stable operation. The switching power stage requires particular attention. Follow these guidelines for good PC board layout:

1) MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise, which results in over-voltage stress on devices. Careful component placement layout and printed circuit design can minimize the voltage spikes induced in the converter. Consider, as an example, the turn-off transition of the upper MOSFET prior to turn-off, the upper MOSFET was carrying the full load current. During turn-off, current stops flowing in the upper MOSFET and is picked up by the low side

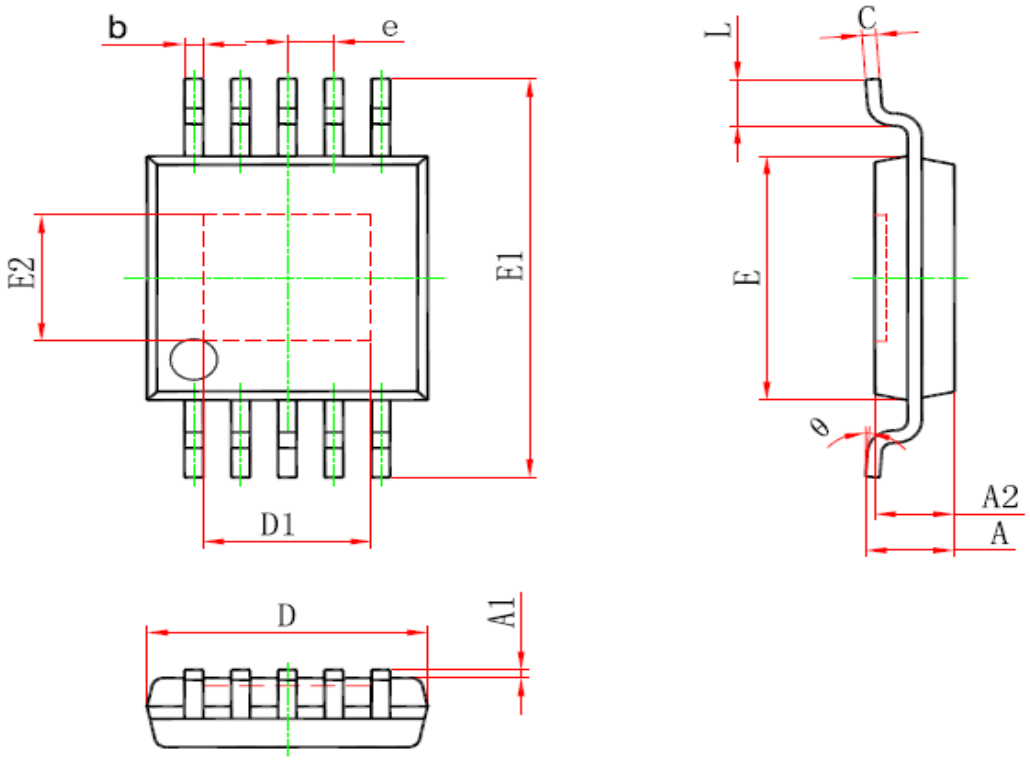
MOSFET or schottky diode. Any inductance in the switched current path generates a large voltage spikes during the switching interval. Careful component selections, layout of the critical components, and use shorter and wider PCB traces help in minimizing the magnitude of voltage spikes.

2) There are two set of critical components in a DC-DC converter using the AAP6150A. The switching power components are most critical because they switch large amounts of energy, and as such, they tend to generate equally large amounts of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bypass current.

3) The power components and the PWM controller should be placed firstly. Place the input capacitors, close to the power switches. Place the output inductor and output capacitors between the MOSFETs and the load. Also locate the PWM controller nearby MOSFETs.

4) If possible, a multi-layer printed circuit board is recommended. The capacitor C_{IN} and C_{OUT} each of them represents numerous capacitors of input and output. Use a dedicated grounding plane and use vias to ground all critical components to this layer. Apply another solid layer as power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the PHASE node is subjected to very high dV/dt voltages, the stray capacitance formed between these islands and the surrounding circuitry will tend to couple switching noise. Use the remaining printed circuit layers for small signal routing. The PCB traces between the PWM controller and the gate of MOSFET and also the traces connecting source of MOSFETs should be sized to carry 2A peak currents.

PACKAGE OUTLINE



MSOP10 PACKAGE OUTLINE AND DIMENSIONS

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
D1	1.700	1.900	0.067	0.075
e	0.50 (BSC)		0.020(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
E2	1.450	1.650	0.057	0.065
L	0.400	0.800	0.016	0.028
θ	0°	6°	0°	6°